Exercise 4 - Notes

Sonntag, 19. Juni 2022 21:53

Exercise (SS 2022)

Comunication Systems and Protocols

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Task 1: Serial Interface

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In the figure 1.1 the pulse diagram of a RS232 interface is given. Different transmission frames have been used for the communication. A transmission frame is composed of a start bit ('0'), 5-8 data bits, no (N, none) or one bit for even (E, even) or odd (O, odd) parity, as well as at least 1 or 2 stop bits (‚1'). Possible frame formats are [5..8][N,O,E][1,2], for example 8N1 for 8 data bits, no parity bit and at least 1 stop bit.

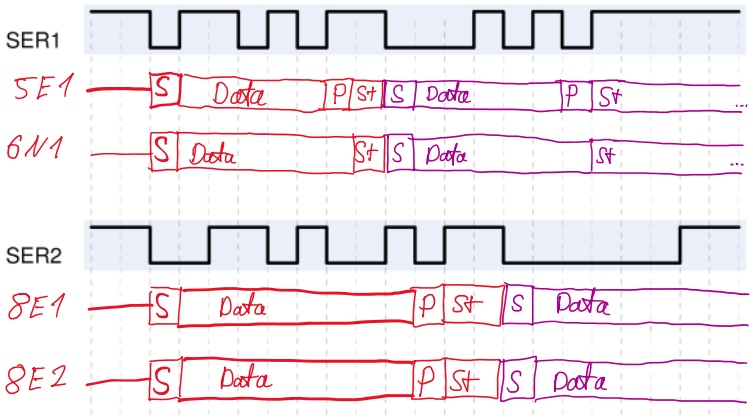

Figure 1.1: Serial interface pulse diagram

1.1 Give all possible frame formats for the pulse sequences as shown in figure 1.1. All given pulse sequences are describing a correct transmission. Start of a transmission is always the startbit in the third timestep.

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1.2 In the figure below different pulse sequences for a RS232 interface are given. Derive from the figure and the given frame formats if the transmission was error free. Mark the erroneous parts in the pulse diagrams.

/2

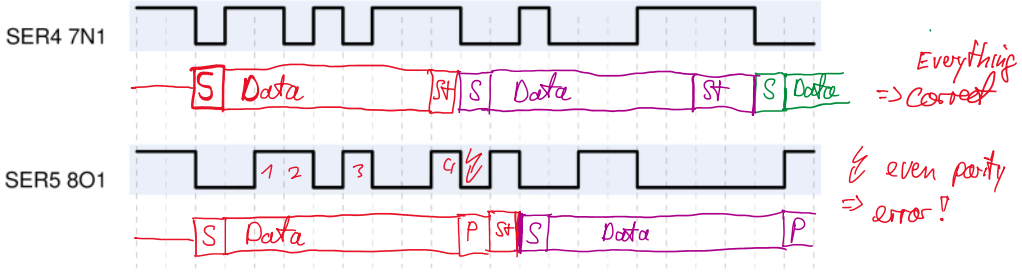

Figure 1.2: RS232 pulse sequences

1.3 Is it possible to detect errors without knowing the frame formats?

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- Not in general.
- Frame format gives position of parity bit.
- Ambigous transmissions possible.

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Task 2: Flow-Control

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A communication system is given in Figure 2.1. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a Level-triggered Closed-loop Flow Control corresponding to Figure 3.1 for the high-level synchronization.

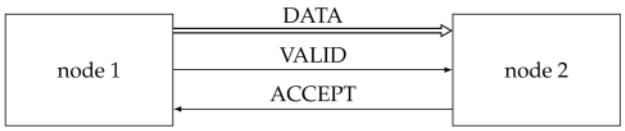

Figure 2.1: Level-triggered Closed-loop Flow Control

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2.1 In Figure 2.2 the sensitive clock edges of the sender and the receiver as well as the signal values for the first sender clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the valid signal is set to '1' by the sender. The receiver will also set the accept signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale.

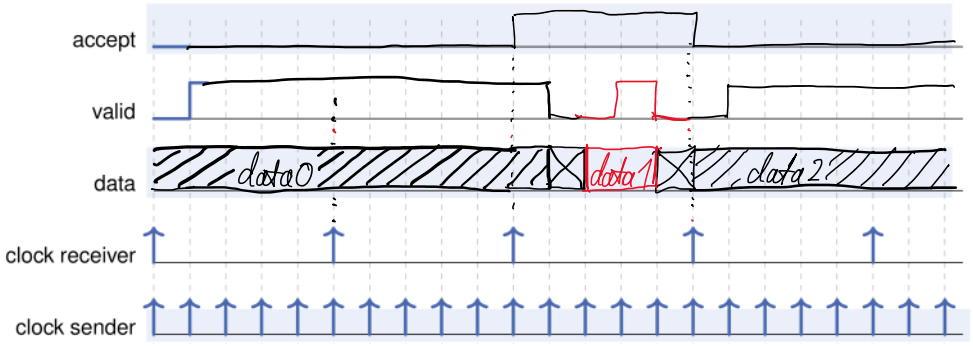

Figure 2.2: Signal progression diagram

/1

2.2 Is this kind of synchronization free from error in this specific case? Justify your answer.

/1

2.3 Propose a better solution for this communication scenario.

2.2: No, data1 gets lost.

2.3: - Synchronise clocks to same frequency
- wait for period after ACK has been received
- Apply edge triggered closed-loop flow control.

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Task 3: Cyclic Redundancy Check

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To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

3.1 Determine the bit string that is associated with the generator polynomial. /1

101

3.2 What is the length of the checksum that is to be appended to the data stream? /1

len (g(x)) = 2

3.3 Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101. /2

Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 1001010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

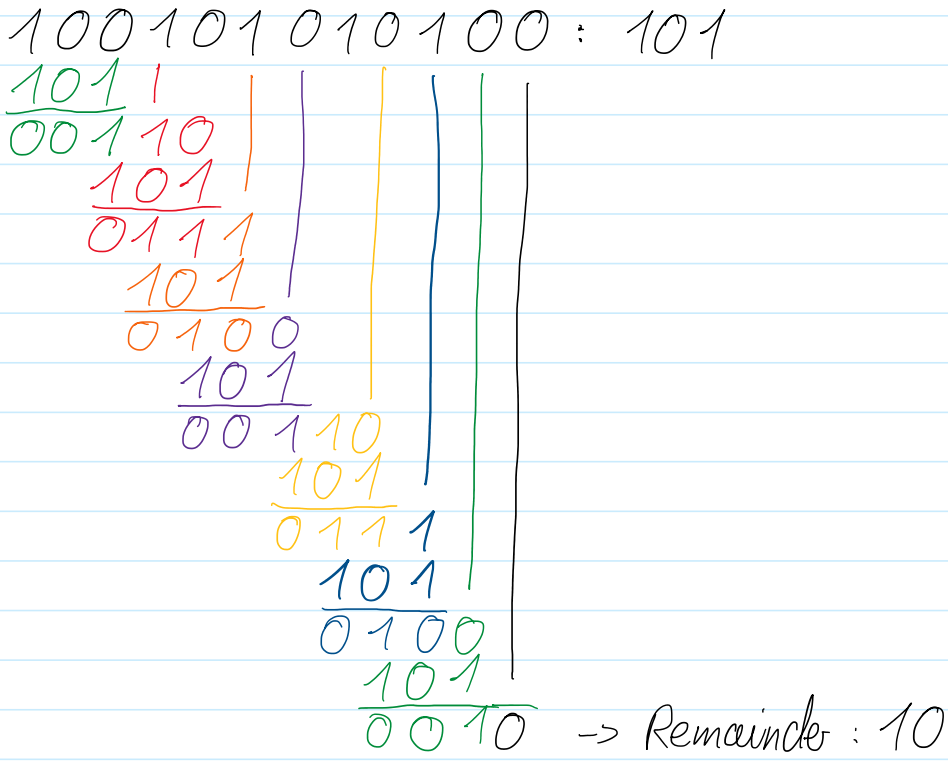
3.4 Denote the bit stream as it arrives at the receiving node. /1

3.5 Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used. /2
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

Hardware Implementation

3.6 To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$). /1

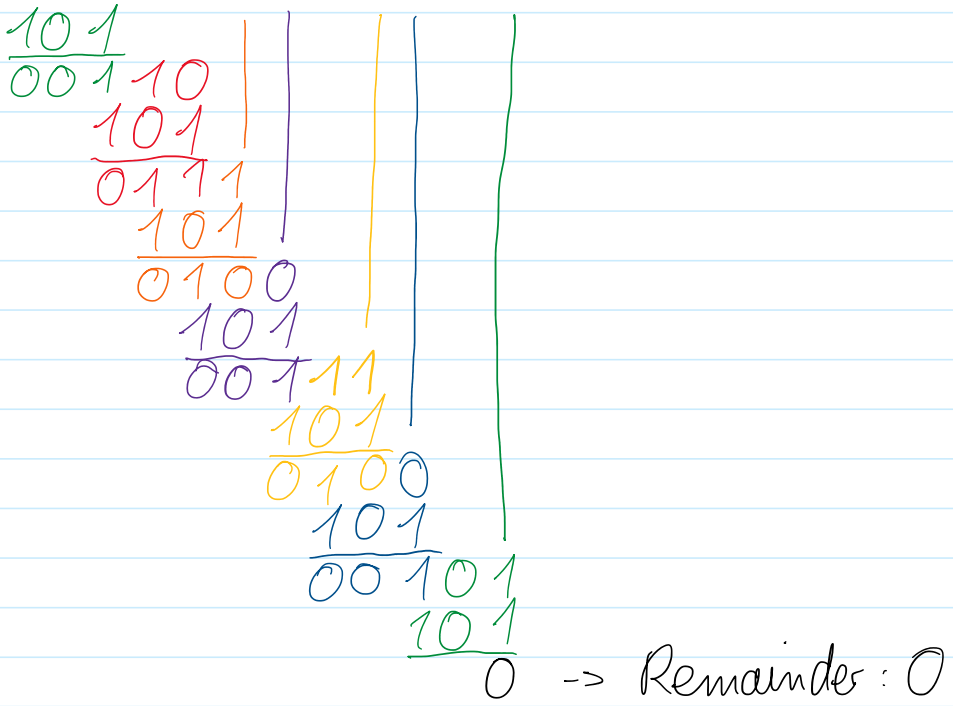
3.3



=> Transmitted: 10010101010

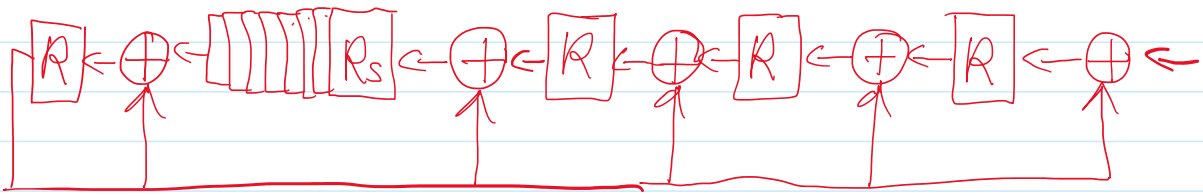
3.4 Received: 10010101001

3.5



=> Receiver thinks transmission is error free

3.6



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Task 4: Error Protection

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Cyclic Redundancy Check (CRC) - Exam Question

4.1 Does the CRC scheme based on the generator polynomial $G(x) = (x + 1)(x^2 + 1)$ allow a receiver to detect all error patterns with exactly three erroneous bits? Justify. /2

Yes, because (x+1) is factor, every odd numbe can be detected.

4.2 The receiver of a CRC-protected message performs the CRC error detection procedure and calculates a non-zero remainder. What can it reliably conclude with respect to the occurrence of a transmission error? /2

Error occured

4.3 Two nodes use the generator polynomial $G(x) = x^4 + x + 1$ to exchange CRC-protected messages. To transmit a certain message, the sender calculates the corresponding checksum, appends this checksum to the raw message, and finally transmits the bit string /3

0010 1110 1010 0011.

Due to transmission errors, however, the recipient receives the bit string

0010 1000 0010 0011.

Is the receiver, who is aware of $G(x)$, able to detect this error? Justify your answer based on the error pattern and the specific error detection capabilities of $G(x)$.

Hint: *Do not perform the calculation that the receiver has to perform to detect errors!*

The error can be detected.

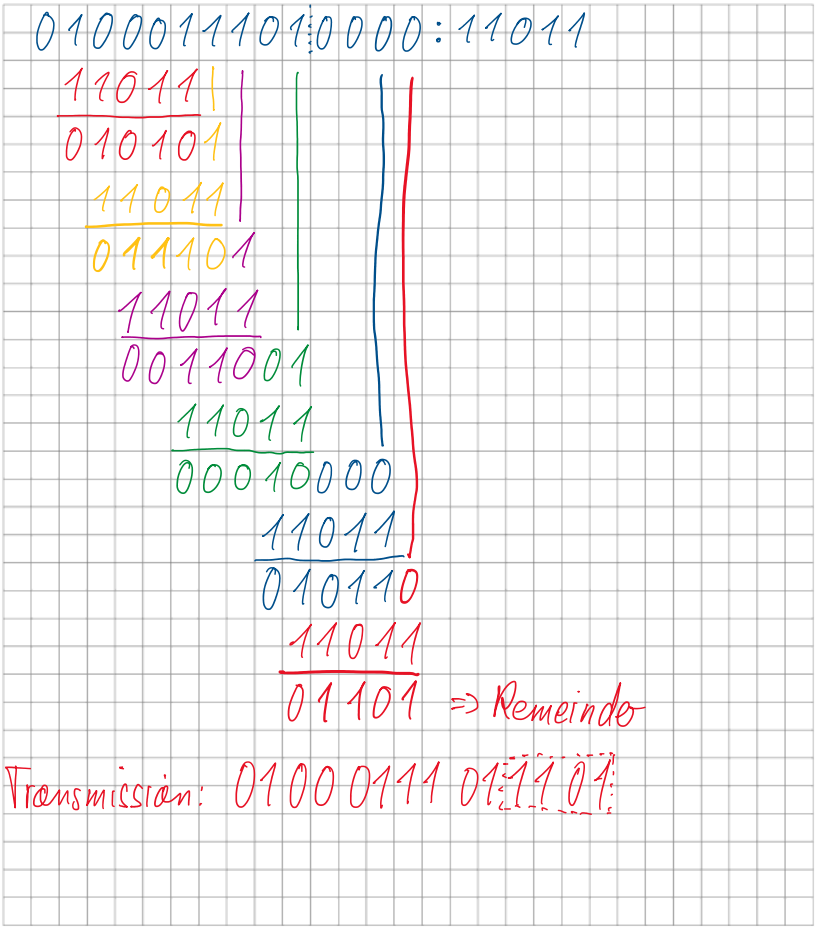
len(e) = len(G(x))

4.4 Given the generator polynomial $G(x) = x^5 + x^4 + 1$, what calculation does the receiver of the CRC-protected bit string "1111 0110 0001" perform as part of its error detection procedure? Give both the dividend and the divisor of this calculation as a bit string. /3

Hint: *This question does not require you to perform the calculation!*

Calculation of 1111 0110 0001 : 110001 is done.

4.5 To transmit it over a channel, the message "0100 0111 01" shall be protected by a CRC checksum. Using the generator polynomial $G(x) = x^4 + x^3 + x + 1$, calculate this checksum and give the bit string that is sent to the receiver. /6



4.6 Give the CRC generator polynomial that is implemented by the linear feedback shift register shown in Figure 4.1. /3

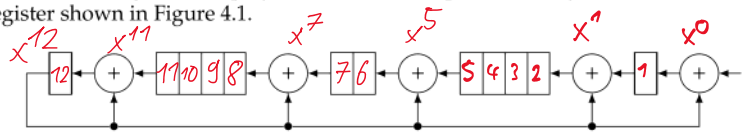


Figure 4.1: Simplified shift register implementation of a CRC scheme

$G(x) = x^{12} + x^{11} + x^7 + x^5 + x + 1$